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10/622,247	07/18/2003	Sheldon C. P. Lim	CS01-150	3131
31366 7590 07/11/2008 HORIZON IP PTE LTD 7500A Beach Road #04-306/308 The Plaza SINGAPORE 199591, SINGAPORE				
EXAMINER HUYNH, PHUONG				
ART UNIT 2857		PAPER NUMBER		
NOTIFICATION DATE 07/11/2008		DELIVERY MODE ELECTRONIC		

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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### Office Action Summary

**Application No.**

10/622,247

**Applicant(s)**

LIM, SHELDON C. P.

**Examiner**

PHUONG HUYNH

**Art Unit**

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 14 March 2008.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-10, 12-27 and 30-35 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 7-10 and 12-22 is/are allowed.
- 6) ☒ Claim(s) 1-6, 23-26 and 30-35 is/are rejected.
- 7) ☒ Claim(s) 27 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_

**DETAILED ACTION**

***Claim Rejections - 35 USC § 103***

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-6, 23, 24, and 31-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Borden et al. (hereinafter "Borden") (US Patent No. 6,049,220) in view of Akram et al. (hereinafter "Akram") (US Patent No. 6,022,750).

Regarding claim 1, Borden discloses a test method comprising:

a) obtaining test measurement values on a device at one or more independent variable values [see Borden: col. 18, line 61-col. 19, line 21];

b) calculating a goodness of fit value for a fitted curve between:

(1) said test measurement values; and

(2) the independent variable values; wherein the goodness of fit value comprises an evaluation of difference between predicted values and test measurement values obtained [see Borden: col. 18, line 61-col. 19, line 21 and lines 38-50]; and using said goodness of fit value to monitor processes used to form said device [see Borden: col. 20, line 50-col. 21, line 4; and col. 8, lines 12-32].

However, Borden does not disclose "providing a first, second and third test structure each having a respective first, second and third test structure parameter".

Further, as said above, Borden discloses "obtaining test measurement values on a device at one or more independent variable values [see Borden: col. 18, line 61-col. 19, line 21]; b) calculating a goodness of fit value for a fitted curve between: (1) said test measurement values; and (2) the independent variable values [see Borden: col. 18, line 61-col. 19, line 21 and lines 38-50]" but not "obtaining from each of the first, second and third test structure at least one test measurement value, the test measurement values varying based on the first, second and third test structure parameter," and not "calculating a goodness of fit value for a fitted curve between said test measurement values and values on the first, second and third test structure parameter" (emphasis added).

Akram teaches "providing a first, second and third test structures on a wafer, each having a respective first, second and third test structure parameter [see Akram: Abstract; col. 3, lines 1-10]" and "obtaining from each of the first, second and third test structure at least one test measurement value, the test measurement values varying based on the first, second and third test structure parameter [see Akram: col. 2, lines 2-17; and col. 5, lines 1-17 and col. 6, lines 1-22] "

Therefore, it would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the invention of Borden to provide a first, second and third test structures and its measurements, as taught by Akram, to obtain various electrical characteristics of the interconnect to be monitored with the interconnect [see Akram: Abstract; col. 5, lines 1-17].

Regarding claim 2, Borden and Akram discloses everything as applied above [see claim 1]. In addition, Borden discloses wherein step (c) further includes using control limits on the goodness of fit values; using said goodness of fit value to (1) control the processes used to form said device or (2) or screen the device [see Borden: col. 17, lines 52-65 and col. 16, lines 3-20 and lines 49-67].

Regarding claim 3, Borden and Akram discloses everything as applied above [see claim 1]. In addition, Borden discloses wherein step (c) further includes using control limits on the goodness of fit values; said control limits established based on a history of goodness of fit values or on device requirements; and using said goodness of fit value to (1) control the process used [see Borden: col. 16, lines 3-20 and lines 49-67].

Regarding claim 4, Borden and Akram discloses everything as applied above [see claim 1]. In addition, Borden discloses the goodness of fit value is a correlation coefficient or a standard error measurement [see Borden: col. 18, lines 31-44].

Regarding claim 5, Borden and Akram discloses everything as applied above [see claim 1]. In addition, Borden discloses the fitted curve is a least squares fitted straight lines [see Borden: col. 4, lines 44-56].

Regarding claim 6, Borden and Akram discloses everything as applied above [see claim 1]. In addition, Borden discloses the test measurement values are resistance

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or capacitance measurement values, and step (c) further comprises using said goodness of fit value to (1) control the processes used to form said device or (2) screen the device [see Borden: col. 22, lines 59-col. 23, line 13 and col. 20, line 50-col. 21, line 4; and col. 8, lines 12-32].

Regarding claim 23, Borden discloses a test method comprising:

measuring test parameter values on the test structure [see Borden: col. 18, line 61-col. 19, line 21];

calculating a goodness of fit value for a fitted curve between: the test parameter values and a dimensional measurement of the test structures; wherein the goodness of fit value is based on an evaluation of difference between predicted values and test parameter values [see Borden: col. 18, line 61-col. 19, line 21 and lines 38-50];

using said goodness of fit value to control the process used to form the device structure or screen the device structure [see Borden: col. 20, line 50-col. 21, line 4; and col. 8, lines 12-32].

Borden discloses "measuring test parameter value on the test structure, calculating a goodness of fit value for a fitted curve between the test parameter values and a dimensional measurement of the test structure" but not "measuring test parameter value on the test structures, calculating a goodness of fit value for a fitted curve between the test parameter values and a dimensional measurement of the test structures" nor "providing a device structure that has at least a first test structure, a

second test structure and a third test structure from which a test parameter is measured" (emphasis added).

Akram teaches "providing a device structure that has at least a first test structure, a second test structure and a third test structure on the substrate from which a test parameter is measured [see Akram: Abstract; col. 3, lines 1-10]" and "measuring test parameter value on the test structures [see Akram: col. 2, lines 2-17; and col. 5, lines 1-17 and col. 6, lines 1-22]."

Therefore, it would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the invention of Borden to provide a first, second and third test structures and its measurements, as taught by Akram, to obtain various electrical characteristics of the interconnect to be monitored with the interconnect [see Akram: Abstract; col. 5, lines 1-17].

Regarding claim 24, Borden and Akram discloses everything as applied above [see claim 23]. In addition, Borden discloses that wherein said test parameter is resistance or capacitance [see Borden: col. 22, lines 59-col. 23, line 13 and col. 20, line 50-col. 21, line 4; and col. 8, lines 12-32].

Regarding claim 31, Borden and Akram discloses everything as applied above [see claim 1]. In addition, Borden discloses that the test measurement values are obtained at two or more test conditions on the device [see Borden: col. 2, lines 34-43].

Regarding claim 32, Borden does not disclose that wherein the first, second and third test structure parameter comprises at least one of length or width of a resistive portion of the respective first, second and third test structure.

Akram teaches that wherein the first, second and third test structure parameter comprises at least one of length or width of a resistive portion of the respective first, second and third test structure [see Akram: col. 6, lines 1-22: area is known hence length and width must be known].

It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the invention of Borden to include the length or width, as taught by Akram, to determine a specific contact resistance [see Akram: col. 6, lines 1-22].

Regarding claim 33, Borden does not disclose wherein the first, second and third test structure parameter comprises an area of a capacitive portion of the respective first, second, and third test structure.

Akram teaches wherein the first, second and third test structure parameter comprises an area of a capacitive portion of the respective first, second, and third test structure [see Akram: col. 6, lines 1-22].

It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the invention of Borden to include the length or width, as taught by Akram, to determine a specific contact resistance [see Akram: col. 6, lines 1-22].

Regarding claim 34, Borden and Akram discloses everything as applied above [see claim 1]. In addition, Borden discloses wherein the test measurement values comprises resistance or capacitance [see Borden: [see Borden: col. 22, lines 59-col. 23, line 13 and col. 20, line 50-col. 21, line 4; and col. 8, lines 12-32].

3. Claim 30 is rejected under 35 U.S.C. 103(a) as being unpatentable over Borden et al. (hereinafter "Borden") (US Patent No. 6,049,220) in view of Akram et al. (hereinafter "Akram") (US Patent No. 6,022,750) as applied to claim 1 above, and further in view of Peng et al. (hereinafter "Peng") (US Patent No. 5,787,190).

Regarding claim 30, Borden and Akram do not disclose that the test measurement values are obtained on two of more test sites on the device.

Peng teaches that the test measurement values are obtained on two of more test sites on the device [see Peng: col. 3, lines 31-60].

It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the invention of Borden in view of Akram, to include the test measurement values obtained from different test sites, as taught by Peng, to obtain different set of test criteria to semiconductor wafers to produce another representative wafer map such as testing for logic defects on a die during the manufacturing process to generate a representative wafer map illustrating defective die pattern on that

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semiconductor wafer or performs component tests to verify the electrical test structure on scribe lines [see Peng: col. 3, lines 31-60].

4. Claims 25, 26, 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Borden et al. (hereinafter "Borden") (US Patent No. 6,049,220) in view of Takekoshi et al. (hereinafter "Takekoshi") (US Patent No. 7,091,733).

Regarding claim 25, Borden discloses a test method comprising:

a) providing a device structure on a wafer that has at least a first test structure [see Borden: col. 8, lines 32-53];

b) measuring a first test measurement on at least the first test structure; [see Borden: col. 8, line 63-col. 9, line 17], **but not a second test measurement, and a third test measurement** on at least the first test structure (emphasis added);

c) calculating a goodness of fit value for a fitted curve between: (1) said test measurement values; and (2) the independent variable values or the first test measurement performed under a first test condition, wherein the goodness of fit value is based on an evaluation of difference between predicted values and test parameter values measured [see Borden: col. 18, line 61-col. 19, line 21 and lines 38-50]" **but not** "the first test measurement performed under a first test condition and (2) the second test measurement performed under a second test condition; (3) the third test measurement performed under a third test condition" (emphasis added);

d) using said goodness of fit value to (1) control processes used to form the device structure or (2) screen the device structure [see Borden: col. 20, line 50-col. 21, line 4; col. 8, lines 12-32; col.21, lines 18-64].

Takekoshi teaches "a device structure on a wafer that have a plurality of test structures", "measuring a second test measurement, and a third test measurement on at least the first test structure" [see Takekoshi: col. 6, lines 30-32; lines 54-57]; "the second test measurement performed under a second test condition; and the third test measurement performed under a third test condition" [i.e. at different temperatures such as within a range of 160C and 350C, or at different supplied current] [see Takekoshi: col. 9, lines 10-25; and col. 15, lines 14-30, lines 30-39].

It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the invention of Borden to include the measurements, as taught by Takekoshi, for evaluating reliabilities of a multilayered interconnection and an insulting film, which are formed on a semiconductor wafer, under an accelerated condition [see Takekoshi: col. 2, lines 54-57; col. 9, lines 10-25; and col. 15, lines 14-30, lines 30-39].

Regarding claim 26, Borden does not disclose that wherein said first test condition, said second test condition, and said third test condition are different temperatures.

Takekoshi teaches wherein said first test condition, said second test condition, and said third test condition are different temperatures [see Takekoshi: col. 2, lines 54-57; col. 9, lines 10-25; and col. 15, lines 14-30, lines 30-39].

It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the invention of Borden to include the measurements, as taught by Takekoshi, for evaluating reliabilities of a multilayered interconnection and an insulting film, which are formed on a semiconductor wafer, under an accelerated condition [see Takekoshi: col. 2, lines 54-57; col. 9, lines 10-25; and col. 15, lines 14-30, lines 30-39].

Regarding claim 35, Borden discloses a method of forming a device comprising: providing a device structure on a wafer that has a first test structure with a test structure parameter [see Borden: col. 8, lines 32-53]; obtaining test measurement value which are based on the test structure parameter[see Borden: col. 8, line 63-col. 9, line 17]; determining a goodness of fit value based on difference between predicted values fitting a curve from test measurement value obtained [see Borden: col. 18, line 61-col. 19, line 21 and lines 38-50; and screening wafers on which devices are formed based on a scrap limit established from the goodness of fit value [see Borden: col. 20, line 50-col. 21, line 4; col. 8, lines 12-32; col.21, lines 18-64]..

Borden discloses providing a device structure on a wafer that has at least a first test structure [see Borden: col. 8, lines 32-53]; but not “providing test structures on a wafer, the test structures having respective test structure parameters”; and “test measurement values”.

Takekoshi teaches providing test structures on a wafer, the test structures having respective test structure parameters”; and “test measurement values” [see Takekoshi: col. 6, lines 30-32; lines 54-57].

It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the invention of Borden to include the measurements, as taught by Takekoshi, for evaluating reliabilities of a multilayered interconnection and an insulting film, which are formed on a semiconductor wafer, under an accelerated condition [see Takekoshi: col. 2, lines 54-57; col. 9, lines 10-25; and col. 15, lines 14-30, lines 30-39].

***Allowable Subject Matter***

Claim 27 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 7-10, 12-22 are allowed [Please see Office Action mailed on April 12, 2007].

***Response to Arguments***

5. Applicant's arguments filed on 03/14/2008 have been considered but are not persuasive.

Regarding amended claims 1, 23 and 25, Applicant argues that Borden in view of Akram or in view of Takekoshi do not disclose the amended claims 1, 23, and 25 [see Applicant's Remarks: Page 10-14]. Accordingly, the amended claims 1, 23 and 25 are disclosed by Borden in view of Akram or in view of Takekoshi [see the above rejections in this office action].

For new claim 35, please also see the above rejections in this office action.

***Conclusion***

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

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the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phuong Huynh whose telephone number is 571-272-2718. The examiner can normally be reached on M-F: 8:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eliseo Ramos-Feliciano can be reached on 571-272-7925. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Phuong Huynh/  
Examiner, Art Unit 2857  
July 4, 2008

/Eliseo Ramos-Feliciano/  
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